**WHAT IS CLAIMED IS:**

1. A method of generating a switching sequence for an unary array of conducting branches of a thermometrically decoded digital-to-analog converter, the conducting branches of which are affected by an error distributed over the array according to a certain error distribution function, comprising the steps of:

preliminary evaluating said error distribution function, fixing an upper bound function and a lower bound function symmetrical to each other of the INL error function associated to the switching sequence, determining the center of gravity of the array and calculating, by said preliminarily evaluated error distribution function, error values associated to each pair of conducting branches symmetrical in respect to the center of gravity of the array;

choosing pairs of successive conducting branches in the switching sequence such that every even conducting branch (2n) is substantially symmetrical to the preceding odd conducting branch (2n-1) in respect to said center of gravity;

building a switching sequence with an INL error function comprised between said upper bound and lower bound functions by:

a) starting from a first chosen pair of conducting branches (1, 2) of the switching sequence iteratively performing the following steps from b1) to b3) for all other pairs of conducting branches of the array:

b1) calculating a corresponding value of the INL error function of the switching sequence being built,

b2) choosing as the successive pair, the pair of conducting branches that maximizes or minimizes the next value of the INL error function of the switching sequence though remaining comprised between the corresponding values of said upper bound and lower bound functions,

b3) if all said other pairs do not meet the conditions of point b2), then repeating the steps from a) to b3) choosing every time a different first pair of branches, and if the conditions cannot yet be met, changing at least one of said bound functions and restarting from point a);

c) when all other pairs of conducting branches of the unary array meet the conditions, outputting the resulting switching sequence.

2. The method of claim 1, further comprising the operations of:

repeating the steps from a) to c) for all possible first pairs of conducting branches using the same bound functions, obtaining a set of switching sequences whose INL error function is comprised between said bound functions;

choosing the switching sequence of said set that satisfies a pre-established criterion.

3. The method of claim 1, wherein said bound functions are constant.

4. The method of claim 3, wherein the value of said upper bound function is half the maximum value of the absolute value of the DNL error affecting the conducting branches of the array.

5. The method of claim 1, wherein said bound functions are closer to 0 in correspondence of mid way values of said switching sequence than in correspondence of the two ends of a range of conversion.

6. The method of claim 2, wherein said criterion consists in choosing the switching sequence of said set that is affected by the smallest absolute INL error.

7. The method of claim 2, wherein said criterion consists in choosing the switching sequence of said set that is affected by the smallest absolute DNL error in correspondence of mid way values of the switching sequence.

8. The method of claim 2, wherein said criterion consists in choosing the switching sequence of said set that is affected by the most evenly oscillating INL error function.

9. The method of claim 1, wherein said pairs of conducting branches are also chosen to make the switching sequence being built anti-symmetrical in respect to an axis of symmetry of the unary array.

10. A thermometrically decoded digital/analog converter, comprising an unary array of conducting branches selectable by respective switches, characterized in that the switching sequence of said branches is generated by using the method of claim 1.

11. A computer program loadable in an internal memory of a computer, comprising a software code for performing the steps of the method of claim 1 when said program is executed on a computer.

12. A method of determining a switching sequence associated with an array of elements, comprising:

choosing a first pair of a plurality of element pairs to be the first and second switched elements in the sequence, each element pair having an associated error value; and

choosing as the third and fourth switched elements in the sequence the element pair having the associated error value that, when added to the first pair error value, yields a first summed error value that is within a predetermined value range defined by upper and lower error tolerance values and that is closest or equal in value to one of the upper and lower error tolerance values.

13. The method of claim 12 wherein each element pair comprises an element having a predetermined relationship with the other element of the pair.

14. The method of claim 13 wherein the predetermined relationship comprises symmetrical positioning with respect to a center of the array.

15. The method of claim 12 wherein the first pair of elements is chosen randomly.

16. The method of claim 12, further comprising:

identifying an element pair having an associated error value that, when added to a summed error value, yields a second summed error value not within the predetermined value range; and

choosing a second pair of the plurality of element pairs to be the first and second switched elements in the sequence.

17. The method of claim 12, further comprising modifying one of the upper and lower error tolerance values.

18. The method of claim 12 wherein the error values comprise integral non-linearity error values.

19. The method of claim 12 wherein the elements comprise current sources.

20. An article of manufacture, comprising: a machine-readable medium having instructions stored thereon to:

choose a first pair of a plurality of arrayed element pairs to be the first and second switched elements in a switching sequence, each element pair having an associated error value; and

choose as the third and fourth switched elements in the sequence the element pair having the associated error value that, when added to the first pair error value, yields a first summed error value that is within a predetermined value range defined by upper and lower error tolerance values and that is closest or equal in value to one of the upper and lower error tolerance values.

21. A system, comprising:

means for choosing a first pair of a plurality of element pairs to be the first and second switched elements in the sequence, each element pair having an associated error value; and

means for choosing as the third and fourth switched elements in the sequence the element pair having the associated error value that, when added to the first pair error value, yields a first summed error value that is within a predetermined value range defined by upper and lower error tolerance values and that is closest or equal in value to one of the upper and lower error tolerance values.

22. A digital-to-analog converter, comprising:

a array of elements comprising a first pair of a plurality of element pairs operable to be chosen as the first and second switched elements in a switching sequence, each element pair having an associated error value; and

a second element pair operable to be chosen as the third and fourth switched elements in the sequence, the second element pair having the associated error value that, when added to the first pair error value, yields a first summed error value that is within a predetermined value range defined by upper and lower error tolerance values and that is closest or equal in value to one of the upper and lower error tolerance values.